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DS64EV400-EVK User Guide
DS64EV400 Programmable Quad Equalizers

Overview

The DS64EV400-EVK evaluation board provides a typical application for the evaluation of the DS64EV400 programmable quad equalizers.

Specifications

DC Input Power (JP1): 3.3V ± 10%, or 2.5V ± 5%

Serial Data Inputs (IN_[0:3] +/-): High-speed CML inputs. Acceptable data input speed DC – 10 Gbps. *For more details, please refer to the datasheet.*

Serial Data Outputs (OUT_[0:3] +/-): High-speed CML outputs. Each output is matched with it's respective input channel. For instance, IN_0+ input routes to OUT_0+. *For more details, please refer to the datasheet.*

CML Input Voltage: -0.5V to 4.0V
CMOS Input Voltage: -0.5V to 4.0V

Jumper Settings

JP2, JP4, JP5, JP6 (SD[0:3] / EN[0:3]): Directly connecting SD and EN at the jumpers provides SD/EN loopback option to detect signal activity and automatically force the equalizer channel into or out of standby mode. By default, the EN [0:3] pins are internally pulled high.

JP3 (EQ_SEL[0:2]/BST[0:2]): These jumpers are control equalization boost levels. Please see Table 1 for equalizer boost control settings.

IMPORTANT ERRATA:
EQUALIZATION SETTINGS JP3 (EQ_SEL[0:2]/BST[0:2]) These pins control the boost level and currently only have the option to be connected to ground using jumpers. In order to select maximum equalization the EQ_SEL[0:2]/BST[0:2] must be hardwired to Vdd. When selecting these EQ settings please use external hardware to force Vdd on these pins.

Table 1. Equalization Boost Controls

6 mil microstrip FR4 trace length (in)	24 AWG Twin-AX cable length (m)	Channel loss at 3.2 GHz	Channel loss at 5 GHz	[BST_2, BST_1, BST_0]
0	0	0 dB	0 dB	0 0 0
5	2	5 dB	6 dB	0 0 1
10	3	7.5 dB	10 dB	0 1 0
15	4	10 dB	14 dB	0 1 1
20	5	12.5 dB	18 dB	1 0 0 (Default)
25	6	15 dB	21 dB	1 0 1
30	7	17 dB	24 dB	1 1 0
40	10	22 dB	30 dB	1 1 1

JP7 (FEB, SDA, and SDC): Connecting FEB pin to GND enables SMBus control pins. By default, the FEB pin is internally pulled high. SDA is serial bus data input, and SDC is serial bus clock input. By default, these pins are internally pulled high.

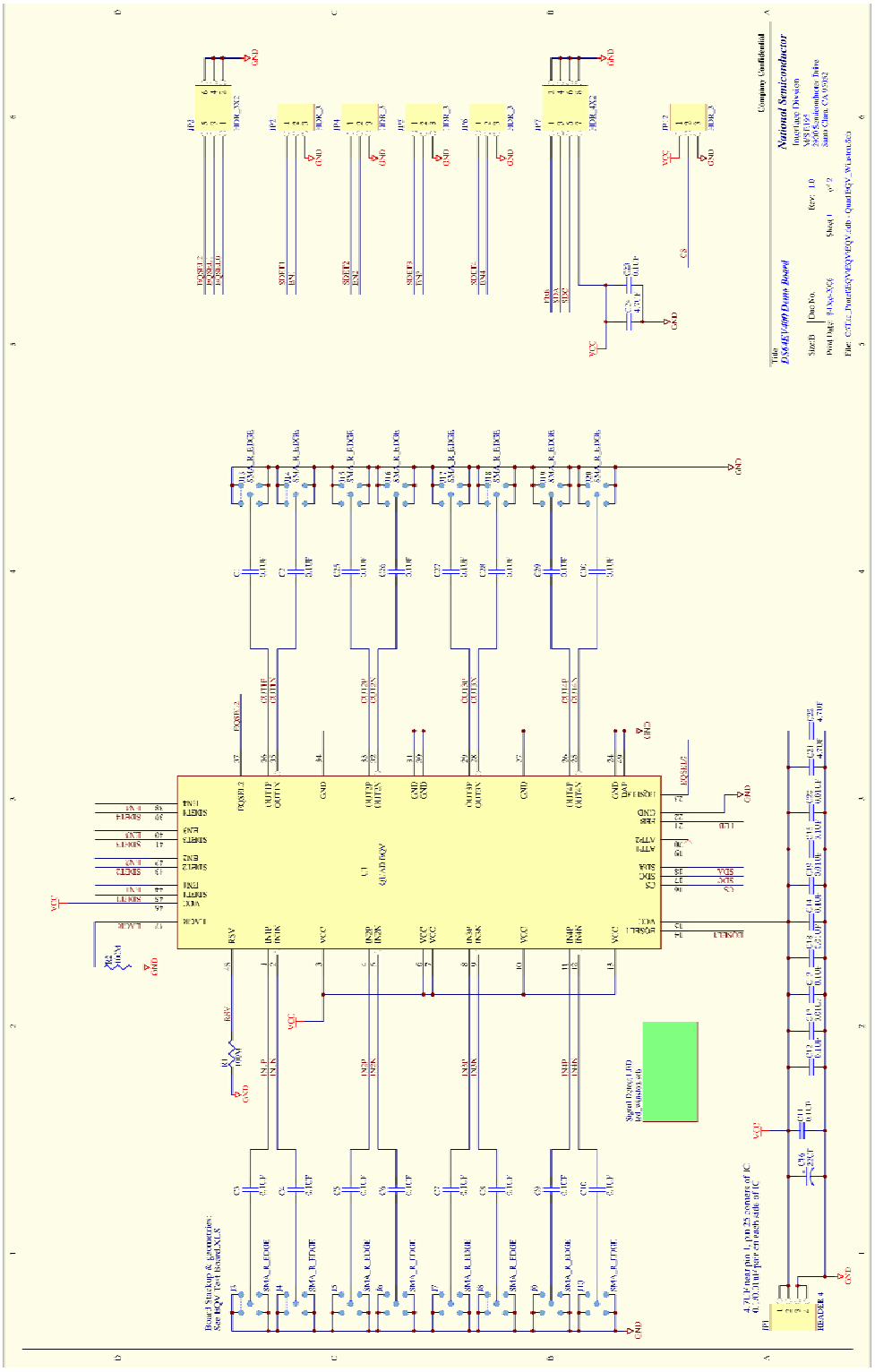
JP8 (CS): Connecting CS pin to high enables the SMBus registers. By default, the CS pinn is internally pulled low.

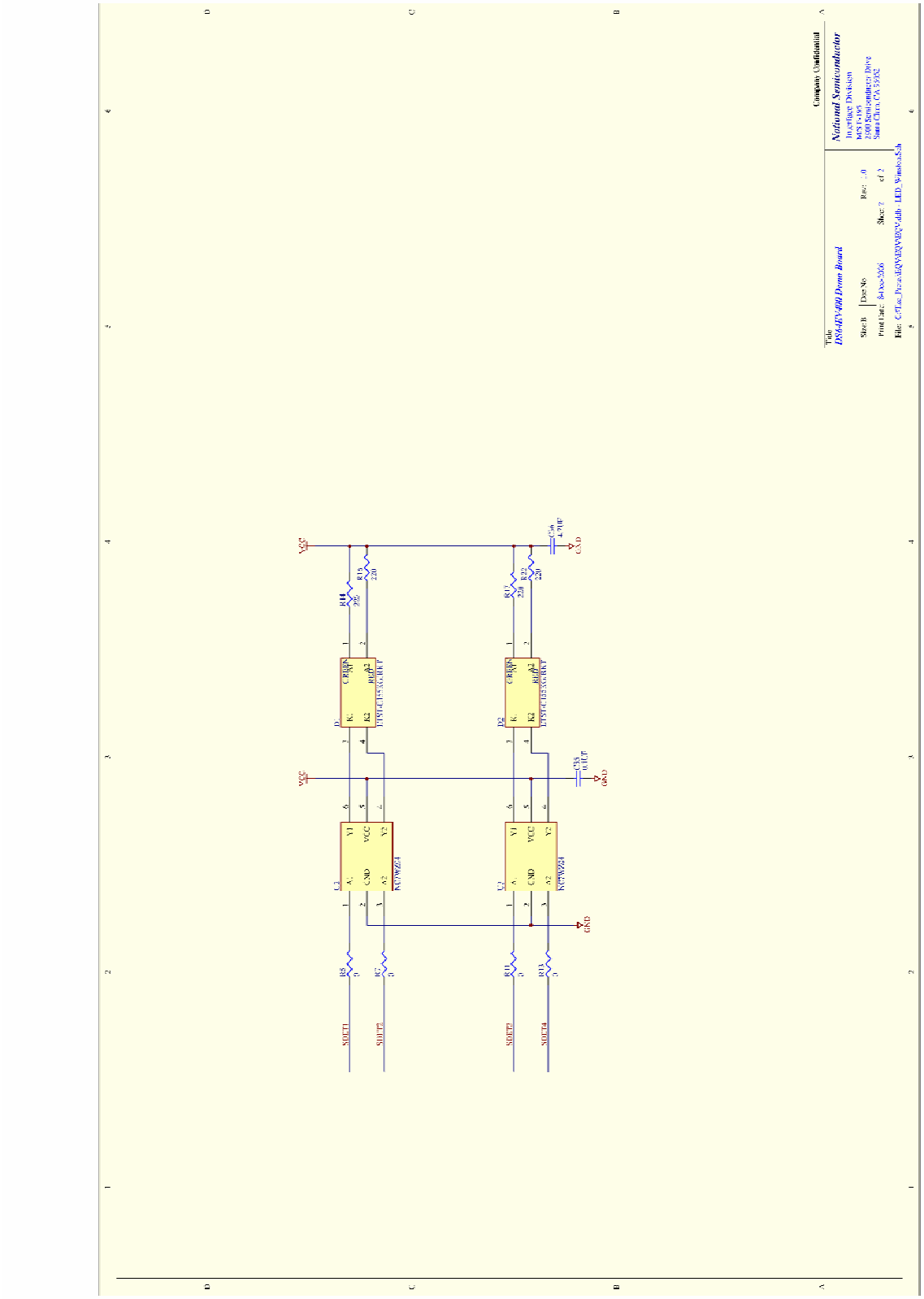
U2, U3, D1, and D2: U2/U3 is NC7WZ04**,** a dual inverter from Fairchild's Ultra High Speed Series of TinyLogic® in the space saving SC70 6-lead package. D1/D2 is a LIST-C155KGJRKT LED lamp. When enabling SD/EN loopback mode by directly connecting SD and EN pins (JP2, JP4, JP5 and JP6), the LED serves as the detecting signaling. When LED is green/red, the SD is not detecting an input signal, and the channel is at a standby mode.

Bill of Materials

DESIGNATION	QTY	DESCRIPTION
C17, C18, C19, C20	4	0.01uF ±10% Ceramic Capacitor 0402
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C23, C25, C26, C27, C28, C29, C30, C35	23	0.1uF ±10% Ceramic Capacitor 0402
C21, C22, C24, C36	4	4.7uF ±10% Ceramic Capacitor 1206
C16	1	22uF ±10% Tan Capacitor 6032
R1, R2	2	Do not populate
R5, R7, R11, R13	4	0 ohm ±5% Resistor 0402
R14, R16, R17, R22	4	220 ohm ±5% Resistor 0603
D1, D2	2	LIST-C155KGJRKT LED lamp
JP1	1	4 Pin Header
JP2, JP4, JP5, JP6, JP12	5	3 Pin Header
JP3	1	3X2 Pin Header
JP7	1	4X2 Pin header
J3, J4, J5, J6, J7, J8, J9, J10, J13, J14, J15, J16, J17, J18, J19, J20	16	SMA Edge Tab Receptacle
U1	1	National DS64EV400
U2, U3	2	Fairchild NC7WZ04

Schematics





Top View Layout